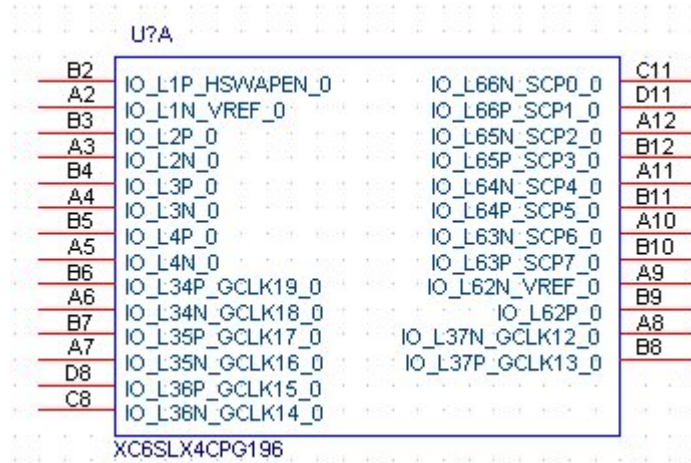


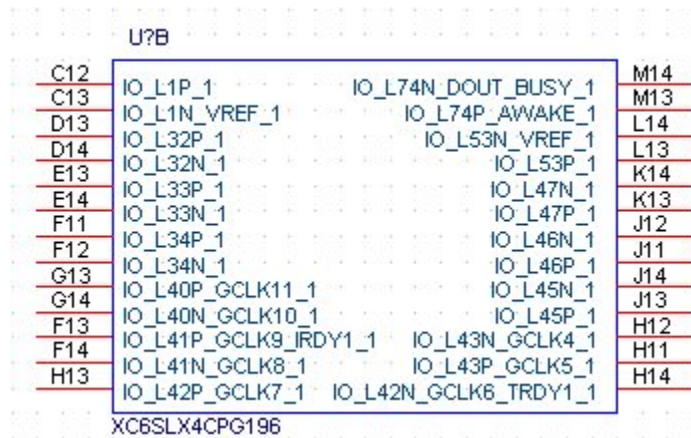
Schematic Symbol for XC6SLX4/LX9/LX16-CPG196

The symbol consists of 6 heterogeneous parts, each of them listed below:

1. I/O Bank 0



2. I/O Bank 1



3. I/O Bank2 (Contains the Programming Interface)

U?C		
M12	CMPCS_B_2	TDO
N14	DONE_2	TMS
N13	IO_L1P_CCLK_2	TDI
P13	IO_L1N_M0_CMPMISO_2	TCK
N12	IO_L2P_CMPCLK_2	
P12	IO_L2N_CMPMOSI_2	SUSPEND
N11	IO_L3P_D0_DIN_MISO_MISO1_2	
P11	IO_L3N_MOSI_CSI_B_MISO0_2	PROGRAM_B_2
N10	IO_L12P_D1_MISO2_2	IO_L65N_CSO_B_2
P10	IO_L12N_D2_MISO3_2	IO_L65P_INIT_B_2
N9	IO_L13P_M1_2	IO_L64N_D9_2
P9	IO_L13N_D10_2	IO_L64P_D8_2
L8	IO_L14P_D11_2	IO_L63N_2
M8	IO_L14N_D12_2	IO_L63P_2
N8	IO_L30P_GCLK1_D13_2	IO_L62N_D6_2
P8	IO_L30N_GCLK0_USERCCLK_2	IO_L62P_D5_2
N7	IO_L31P_GCLK31_D14_2	IO_L49N_D4_2
P7	IO_L31N_GCLK30_D15_2	IO_L49P_D3_2
N6	IO_L48P_D7_2	IO_L48N_RDWR_B_VREF_2

XC6SLX4CPG196

4. I/O Bank 3

U?D		
M2	IO_L1P_3	IO_L83N_VREF_3
M1	IO_L1N_VREF_3	IO_L83P_3
L2	IO_L2P_3	IO_L52N_3
L1	IO_L2N_3	IO_L52P_3
K2	IO_L36P_3	IO_L51N_3
K1	IO_L36N_3	IO_L51P_3
J4	IO_L37P_3	IO_L50N_3
J3	IO_L37N_3	IO_L50P_3
J2	IO_L41P_GCLK27_3	IO_L49N_3
J1	IO_L41N_GCLK26_3	IO_L49P_3
G2	IO_L42P_GCLK25_TRDY2_3	
G1	IO_L42N_GCLK24_3	IO_L44N_GCLK20_3
H2	IO_L43P_GCLK23_3	IO_L44P_GCLK21_3
H1	IO_L43N_GCLK22_IRDY2_3	

XC6SLX4CPG196

5. GND

U?E			
A1	GND	GND	P14
A14	GND	GND	P1
C2	GND	GND	M7
C3	GND	GND	M3
C6	GND	GND	M11
C7	GND	GND	L9
D10	GND	GND	L6
D5	GND	GND	L5
D6	GND	GND	L3
D9	GND	GND	
E11	GND	GND	L11
E8	GND	GND	L10
F7	GND	GND	K8
F8	GND	GND	J8
G4	GND	GND	J7
G5	GND	GND	J10
G6	GND	GND	H9
G7	GND	GND	H8
G8	GND	GND	H7
H10	GND	GND	H4
	GND	GND	

XC6SLX4CPG196

6. Power

U?F			
E10	VCCINT	VCCO_3	K4
E5	VCCINT	VCCO_3	K3
E6	VCCINT	VCCO_3	H3
E9	VCCINT	VCCO_3	G3
F10	VCCINT	VCCO_3	E4
F5	VCCINT	VCCO_3	E3
F6	VCCINT		
F9	VCCINT		
J5	VCCINT	VCCO_2	M9
J6	VCCINT	VCCO_2	M6
J9	VCCINT	VCCO_2	M5
K10	VCCINT	VCCO_2	M10
K5	VCCINT		
K6	VCCINT	VCCO_1	K12
K9	VCCINT	VCCO_1	K11
		VCCO_1	G12
D7		VCCO_1	G11
E7	VCCAUX	VCCO_1	E12
G10	VCCAUX	VCCO_1	D12
G9	VCCAUX	VCCO_1	
H5	VCCAUX		C9
H6	VCCAUX	VCCO_0	C5
K7	VCCAUX	VCCO_0	C4
L7	VCCAUX	VCCO_0	C10
	VCCAUX	VCCO_0	

XC6SLX4CPG196

Notes:

1. The dedicated DONE_2 and PROGRAM_B are powered by Bank2.
2. The JTAG pins and SUSPEND are powered by VCCAUX.
3. When SUSPEND is not used, connect this pin to GND.
4. CMPCS_B_2 –Reserved Input. Connect high or leave unconnected.
5. The following parts in this package are pin for pin compatible: LX4, LX9 and LX16. For details please check the “Spartan 6 Packaging and Pinouts” User Guide that can be found at:
http://www.xilinx.com/support/documentation/user_guides/ug385.pdf

Document Revision History

	Revision	Date	By	Comments
1	1.00	Mar 14, 2010	LD	Initial Release –Uses Xilinx Pinout ASCII File -01/12/2010. Check the Xilinx website for updates.