

Schematic Symbol for XC6SLX4-TQG144

The symbol consists of 3 heterogeneous parts, each of them listed below:

1. I/O Bank 0/1

U?A		
P144	IO_L1P_HSWAPEN_0	IO_L74N_DOUT_BUSY_1
P143	IO_L1N_VREF_0	IO_L74P_AWAKE_1
P142	IO_L2P_0	IO_L47N_1
P141	IO_L2N_0	IO_L47P_1
P140	IO_L3P_0	IO_L46N_1
P139	IO_L3N_0	IO_L46P_1
P138	IO_L4P_0	IO_L45N_1
P137	IO_L4N_0	IO_L45P_1
P134	IO_L34P_GCLK19_0	IO_L43N_GCLK4_1
P133	IO_L34N_GCLK18_0	IO_L43P_GCLK5_1
P132	IO_L35P_GCLK17_0	IO_L42N_GCLK6_TRDY1_1
P131	IO_L35N_GCLK16_0	IO_L42P_GCLK7_1
P127	IO_L36P_GCLK15_0	IO_L41N_GCLK8_1
P126	IO_L36N_GCLK14_0	IO_L41P_GCLK9_IRDY1_1
P124	IO_L37P_GCLK13_0	IO_L40N_GCLK10_1
P123	IO_L37N_GCLK12_0	IO_L40P_GCLK11_1
P121	IO_L62P_0	IO_L34N_1
P120	IO_L62N_VREF_0	IO_L34P_1
P119	IO_L63P_SCP7_0	IO_L33N_1
P118	IO_L63N_SCP6_0	IO_L33P_1
P117	IO_L64P_SCP5_0	IO_L32N_1
P116	IO_L64N_SCP4_0	IO_L32P_1
P115	IO_L65P_SCP3_0	IO_L1N_VREF_1
P114	IO_L65N_SCP2_0	IO_L1P_1
P112	IO_L66P_SCP1_0	
P111	IO_L66N_SCP0_0	

XC6SLX4-TQG144

2. I/O Bank 2/3 (Contains the Programming Interface)

U?B		
P72	CMPCS_B_2	IO_L83N_VREF_3
P71	DONE_2	IO_L83P_3
P70	IO_L1P_CCLK_2	IO_L52N_3
P69	IO_L1N_M0_CMPMISO_2	IO_L52P_3
P67	IO_L2P_CMPCLK_2	IO_L51N_3
P66	IO_L2N_CMPMOSI_2	IO_L51P_3
P65	IO_L3P_D0_DIN_MISO1_2	IO_L50N_3
P64	IO_L3N_MOSI_CSI_B_MISO0_2	IO_L50P_3
P62	IO_L12P_D1_MISO2_2	IO_L49N_3
P61	IO_L12N_D2_MISO3_2	IO_L49P_3
P60	IO_L13P_M1_2	IO_L44N_GCLK20_3
P59	IO_L13N_D10_2	IO_L44P_GCLK21_3
P58	IO_L14P_D11_2	IO_L43N_GCLK22_IRDY2_3
P57	IO_L14N_D12_2	IO_L43P_GCLK23_3
P56	IO_L30P_GCLK1_D13_2	IO_L42N_GCLK24_3
P55	IO_L30N_GCLK0_USERCCLK_2	IO_L42P_GCLK25_TRDY2_3
P51	IO_L31P_GCLK31_D14_2	IO_L41N_GCLK26_3
P50	IO_L31N_GCLK30_D15_2	IO_L41P_GCLK27_3
P48	IO_L48P_D7_2	IO_L37N_3
P47	IO_L48N_RDWR_B_VREF_2	IO_L37P_3
P46	IO_L49P_D3_2	IO_L36N_3
P45	IO_L49N_D4_2	IO_L36P_3
P44	IO_L62P_D5_2	IO_L2N_3
P43	IO_L62N_D6_2	IO_L2P_3
P41	IO_L64P_D8_2	IO_L1N_VREF_3
P40	IO_L64N_D9_2	IO_L1P_3
P39	IO_L65P_INIT_B_2	
P38	IO_L65N_CSO_B_2	TDO
P37	PROGRAM_B_2	TMS
		TDI
P73	SUSPEND	TCK

XC6SLX4-TQG144

3. Power and GND

U?C			
P128	VCCINT	VCCO_3	P4
P19	VCCINT	VCCO_3	P31
P28	VCCINT	VCCO_3	P18
P52	VCCINT	VCCO_3	
P89	VCCINT	VCCO_2	P63
		VCCO_2	P42
P108	GND	VCCO_1	P86
P113	GND	VCCO_1	P76
P13	GND	VCCO_1	P103
P130	GND	VCCO_1	
P136	GND	VCCO_0	P135
P25	GND	VCCO_0	P125
P3	GND	VCCO_0	P122
P49	GND	VCCO_0	
P54	GND	VCCAUX	P90
P68	GND	VCCAUX	P53
P77	GND	VCCAUX	P36
P91	GND	VCCAUX	P20
P96	GND	VCCAUX	P129
	GND	VCCAUX	

XC6SLX4-TQG144

Notes:

1. The dedicated DONE_2 and PROGRAM_B are powered by Bank2.
2. The JTAG pins and SUSPEND are powered by VCCAUX.
3. When SUSPEND is not used, connect this pin to GND.
4. CMPCS_B_2 –Reserved Input. Connect high or leave unconnected.
5. For details please check the “Spartan 6 Packaging and Pinouts” User Guide that can be found at:

http://www.xilinx.com/support/documentation/user_guides/ug385.pdf

Document Revision History

	Revision	Date	By	Comments
1	1.00	Mar 14, 2010	LD	Initial Release –Uses Xilinx Pinout ASCII File -02/22/2010. Check the Xilinx website for updates.