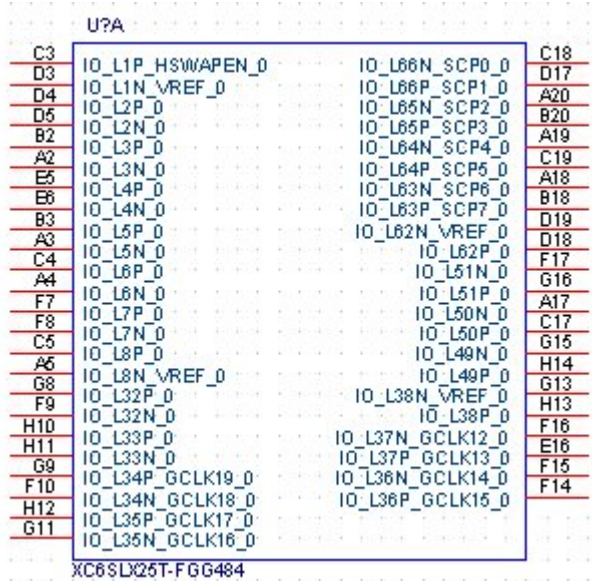


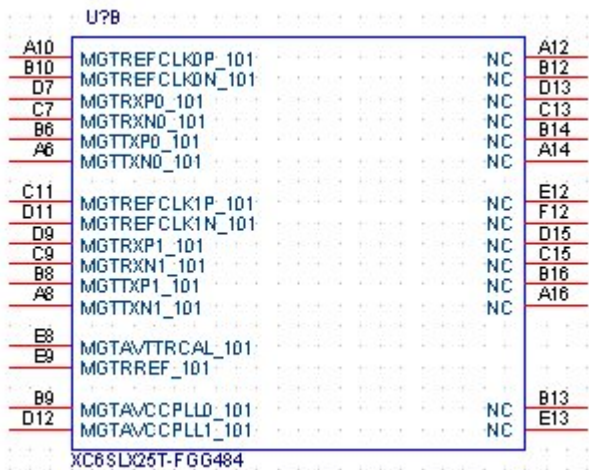
Schematic Symbol for XC6SLX25T-FGG484

The symbol consists of 7 heterogeneous parts, each of them listed below:

1. I/O Bank 0



2. MGT 101 and 123 (BANK0)



3. I/O Bank 1

U?C			
F18	IO_L1P_A25_1	IO_L74N_DOUT_BUSY_1	V20
F19	IO_L1N_A24_VREF_1	IO_L74P_AWAKE_1	V19
H16	NC	NC	T18
H17	NC	NC	T19
B21	NC	NC	T17
B22	NC	NC	R17
J16	NC	NC	P18
J17	IO_L19P_1	NC	P17
C20	IO_L19N_1	NC	R16
C22	IO_L20P_1	NC	R15
L15	IO_L20N_1	NC	M18
K16	NC	IO_L81N_1	M17
D21	NC	IO_L81P_1	P16
D22	NC	IO_L80N_1	N16
G19	NC	IO_L80P_1	T20
F20	IO_L29P_A23_M1A13_1	IO_L59N_1	U19
H18	IO_L29N_A22_M1A14_1	IO_L59P_1	U19
H19	IO_L30P_A21_M1RESET_1	NC	N15
F21	IO_L30N_A20_M1A11_1	NC	M16
F22	IO_L31P_A19_M1CKE_1	IO_L53N_VREF_1	R19
E20	IO_L31N_A18_M1A12_1	IO_L53P_1	P19
E22	IO_L32P_A17_M1A8_1	IO_L52N_M1DQ15_1	Y22
J19	IO_L32N_A16_M1A9_1	IO_L52P_M1DQ14_1	Y21
H20	IO_L33P_A15_M1A10_1	IO_L51N_M1DQ13_1	W22
K19	IO_L33N_A14_M1A4_1	IO_L51P_M1DQ12_1	W20
K18	IO_L34P_A13_M1WE_1	IO_L50N_M1UDQS_N_1	V22
G20	IO_L34N_A12_M1BA2_1	IO_L50P_M1UDQS_1	V21
G22	IO_L35P_A11_M1A7_1	IO_L49N_M1DQ11_1	U22
K17	IO_L35N_A10_M1A2_1	IO_L49P_M1DQ10_1	U20
L17	IO_L36P_A9_M1BA0_1	IO_L48N_M1DQ9_1	T22
H21	IO_L36N_A8_M1BA1_1	IO_L48P_HDC_M1DQ8_1	T21
H22	IO_L37P_A7_M1A0_1	IO_L47N_LDC_M1DQ1_1	R22
K20	IO_L37N_A6_M1A1_1	IO_L47P_FWE_B_M1DQ0_1	R20
L19	IO_L38P_A6_M1CLK_1	IO_L46N_FOE_B_M1DQ3_1	P22
J20	IO_L38N_A4_M1CLKN_1	IO_L46P_FCS_B_M1DQ2_1	P21
J22	IO_L39P_M1A3_1	IO_L45N_A0_M1LDQS_N_1	N22
M20	IO_L39N_M1ODT_1	IO_L45P_A1_M1LDQS_1	N20
M19	IO_L40P_GCLK11_M1A6_1	IO_L44N_A2_M1DQ7_1	M22
K21	IO_L40N_GCLK10_M1A6_1	IO_L44P_A3_M1DQ6_1	M21
K22	IO_L41P_GCLK9_TRDY1_M1RAS_N_1	IO_L43N_GCLK4_M1DQ5_1	L22
P20	IO_L41N_GCLK8_M1CAS_N_1	IO_L43P_GCLK5_M1DQ4_1	L20
	IO_L42P_GCLK7_M1UDM_1	IO_L42N_GCLK6_TRDY1_M1LDM_1	N19

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4. I/O Bank2 (Contains the Programming Interface)

U?D			
V18	CMPCS_B_2	TDO	G17
AB21	DONE_2	TMS	D20
Y20	IO_L1P_CCLK_2	TDI	E18
AA21	IO_L1N_M0_CMPMISO_2	TCK	A21
V17	IO_L2P_CMPCLK_2		
W18	IO_L2N_CMPMOSI_2		
AA20	IO_L3P_D0_DIN_MISO_MISO1_2	SUSPEND	AA22
AB20	IO_L3N_MOSI_CSI_B_MISO0_2	NC	T16
U16	NC	NC	P15
V15	NC	NC	U17
W17	IO_L5P_2		
Y18	IO_L5N_2	PROGRAM_B_2	AB2
AA14	IO_L6P_2	IO_L65N_CSO_B_2	AA3
AB14	IO_L6N_2	IO_L65P_INIT_B_2	Y4
R13	IO_L12P_D1_MISO2_2	IO_L64N_D9_2	U6
T14	IO_L12N_D2_MISO3_2	IO_L64P_D8_2	T7
Y19	IO_L13P_M1_2	IO_L63N_2	AB4
AB19	IO_L13N_D10_2	IO_L63P_2	AA4
AA18	IO_L14P_D11_2	IO_L62N_D6_2	AB5
AB18	IO_L14N_D12_2	IO_L62P_D5_2	Y5
Y17	IO_L15P_2	IO_L60N_2	Y6
AB17	IO_L15N_2	IO_L60P_2	W6
U14	IO_L16P_2	IO_L59N_2	R8
U13	IO_L16N_VREF_2	IO_L59P_2	R9
Y16	IO_L17P_2	IO_L58N_2	W8
W15	IO_L17N_2	IO_L58P_2	V7
V13	IO_L18P_2	IO_L57N_2	U8
W13	IO_L18N_2	IO_L57P_2	T8
AA16	IO_L19P_2	IO_L50N_2	V9
AB16	IO_L19N_2	IO_L50P_2	U9
W14	IO_L20P_2	IO_L49N_D4_2	AB6
Y14	IO_L20N_2	IO_L49P_D3_2	AA6
Y15	IO_L21P_2	IO_L48N_RDWR_B_VREF_2	Y8
AB15	IO_L21N_2	IO_L48P_D7_2	W9
R11	NC	IO_L47N_2	AB7
T11	NC	IO_L47P_2	Y7
T15	NC	IO_L46N_2	U10
U15	NC	IO_L46P_2	T10
T12	IO_L29P_GCLK3_2	IO_L45N_2	AB8
U12	IO_L29N_GCLK2_2	IO_L45P_2	AA8
Y13	IO_L30P_GCLK1_D13_2	IO_L44N_2	Y10
AB13	IO_L30N_GCLK0_USERCCLK_2	IO_L44P_2	W10
AA12	IO_L31P_GCLK3T_D14_2	IO_L43N_2	AB9
AB12	IO_L31N_GCLK30_D15_2	IO_L43P_2	Y9
Y11	IO_L32P_GCLK29_2	IO_L42N_2	W11
AB11	IO_L32N_GCLK28_2	IO_L42P_2	V11
W12	IO_L40P_2	IO_L41N_VREF_2	AB10
Y12	IO_L40N_2	IO_L41P_2	AA10

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6. GND

U?F			
A1	GND	GND	W7
A11	GND	GND	W19
A13	GND	GND	W16
A22	GND	GND	V4
A9	GND	GND	V14
AA13	GND	GND	V10
AA17	GND	GND	U7
AA6	GND	GND	U21
AA9	GND	GND	U2
AB1	GND	GND	R5
AB22	GND	GND	R18
B11	GND	GND	P14
B15	GND	GND	P12
B17	GND	GND	P10
B5	GND	GND	N9
B7	GND	GND	N21
C12	GND	GND	N2
C14	GND	GND	
C16	GND	GND	N17
C6	GND	GND	N13
C8	GND	GND	N11
D10	GND	GND	M14
D16	GND	GND	M12
D6	GND	GND	M10
E11	GND	GND	L9
E14	GND	GND	L5
E15	GND	GND	L18
E2	GND	GND	L13
E21	GND	GND	L11
E7	GND	GND	K14
F13	GND	GND	K12
G18	GND	GND	K10
G5	GND	GND	J9
H7	GND	GND	J21
J11	GND	GND	J2
J13	GND	GND	J15

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Notes:

1. The dedicated pins DONE_2 and PROGRAM_B are powered by Bank2.
2. The JTAG pins and SUSPEND are powered by VCCAUX.
3. When SUSPEND is not used, connect this pin to GND.
4. CMPCS_B_2 –Reserved Input. Connect high or leave unconnected.
5. The following parts in this package have similar but not identical pinout: LX25T, LX45T, LX75T, LX100T and LX150T. If migration between different component densities is desired, please pay attention to the NC pins on each of the devices that are targeted for implementation. For details please check the UG385, “Spartan 6 Packaging and Pinouts” User Guide that can be found at:
http://www.xilinx.com/support/documentation/user_guides/ug385.pdf

Document Revision History

	Revision	Date	By	Comments
1	1.00	Mar 15, 2010	LD	Initial Release –Uses Xilinx Pinout ASCII File -02/22/2010. Check the Xilinx website for updates.