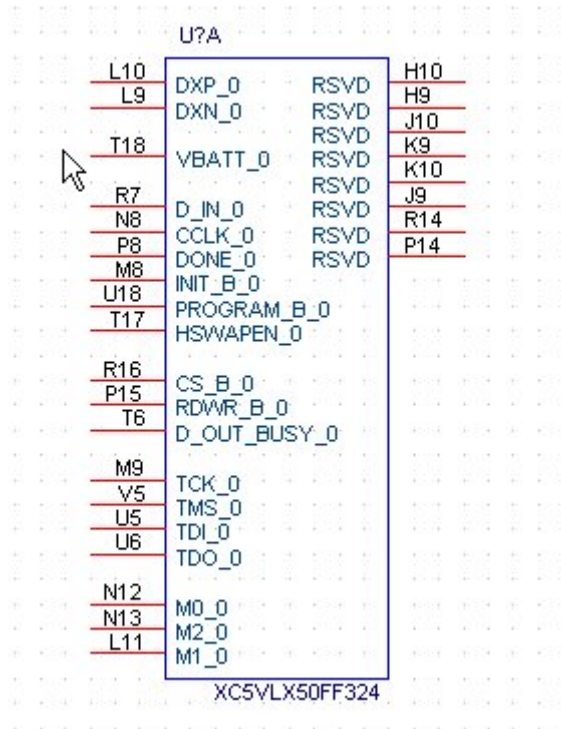


Schematic Symbol for XC5VLX50 FF324

The Schematic symbol consists of 7 heterogeneous parts that are listed below:

1. Programming Interface

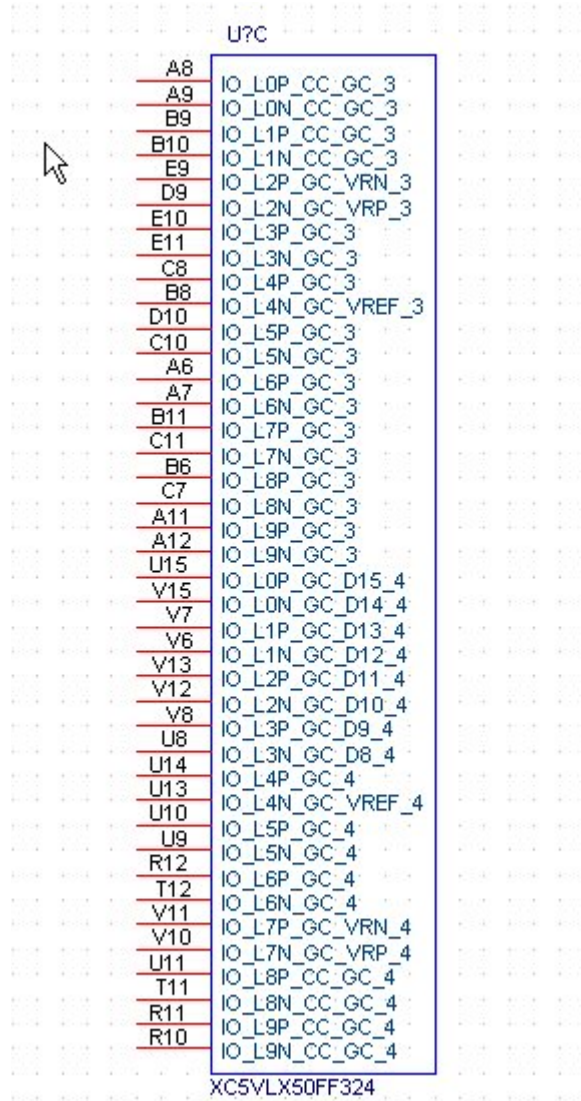


2. I/O Banks 1 and 2

U?B	
F11	IO_L0P_A19_1
G11	IO_L0N_A18_1
G10	IO_L1P_A17_1
F9	IO_L1N_A16_1
E12	IO_L2P_A15_D31_1
D12	IO_L2N_A14_D30_1
F8	IO_L3P_A13_D29_1
G9	IO_L3N_A12_D28_1
C12	IO_L4P_A11_D27_1
D13	IO_L4N_VREF_A10_D26_1
G8	IO_L5P_A9_D25_1
F7	IO_L5N_A8_D24_1
F12	IO_L6P_A7_D23_1
F13	IO_L6N_A6_D22_1
D8	IO_L7P_A5_D21_1
E7	IO_L7N_A4_D20_1
G13	IO_L8P_CC_A3_D19_1
H13	IO_L8N_CC_A2_D18_1
D7	IO_L9P_CC_A1_D17_1
C6	IO_L9N_CC_A0_D16_1
T8	IO_L0P_CC_RS1_2
T7	IO_L0N_CC_RS0_2
R15	IO_L1P_CC_A25_2
T16	IO_L1N_CC_A24_2
R9	IO_L2P_A23_2
T9	IO_L2N_A22_2
V18	IO_L3P_A21_2
V17	IO_L3N_A20_2
P10	IO_L4P_FCS_B_2
P9	IO_L4N_VREF_FOE_B_MOSI_2
U16	IO_L5P_FWE_B_2
V16	IO_L5N_CSO_B_2
N10	IO_L6P_D7_2
M10	IO_L6N_D6_2
T14	IO_L7P_D5_2
T13	IO_L7N_D4_2
N11	IO_L8P_D3_2
M11	IO_L8N_D2_FS2_2
P13	IO_L9P_D1_FS1_2
P12	IO_L9N_D0_FS0_2

XC5VLX50FF324

3. I/O Banks 3 and 4



4. I/O Bank 11

Pin Label	Function
C15	IO_L0P_11
C16	IO_L0N_11
A13	IO_L1P_11
A14	IO_L1N_11
B14	IO_L2P_11
B15	IO_L2N_11
B16	IO_L3P_11
A16	IO_L3N_11
D14	IO_L4P_11
E14	IO_L4N_VREF_11
A17	IO_L5P_11
A18	IO_L5N_11
C13	IO_L6P_11
B13	IO_L6N_11
B18	IO_L7P_11
C17	IO_L7N_11
F14	IO_L8P_CC_11
G14	IO_L8N_CC_11
F16	IO_L9P_CC_11
E16	IO_L9N_CC_11
E17	IO_L10P_CC_11
D17	IO_L10N_CC_11
D15	IO_L11P_CC_11
E15	IO_L11N_CC_11
D18	IO_L12P_VRN_11
C18	IO_L12N_VRP_11
H15	IO_L13P_11
G15	IO_L13N_11
F18	IO_L14P_11
F17	IO_L14N_VREF_11
H16	IO_L15P_11
G16	IO_L15N_11
H18	IO_L16P_11
G18	IO_L16N_11
H17	IO_L17P_11
J17	IO_L17N_11
K17	IO_L18P_11
J18	IO_L18N_11
J15	IO_L19P_11
J14	IO_L19N_11

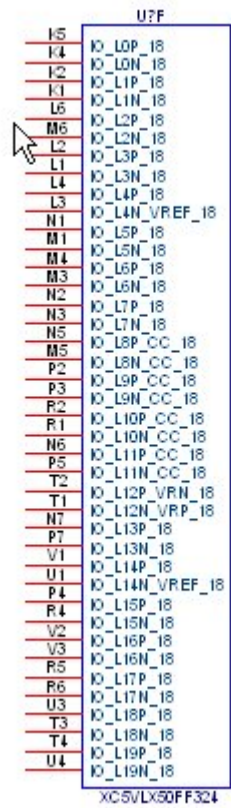
XC5VLX50FF324

5. I/O Banks 12 and 13

U7E	
B5	I0_L0P_12
F6	I0_L0N_12
B5	I0_L1P_12
C5	I0_L1N_12
D5	I0_L2P_12
D4	I0_L2N_12
B4	I0_L3P_12
A4	I0_L3N_12
E5	I0_L4P_12
E4	I0_L4N_VREF_12
A3	I0_L5P_12
B3	I0_L5N_12
G5	I0_L6P_12
G6	I0_L6N_12
C3	I0_L7P_12
D3	I0_L7N_12
H6	I0_L8P_CC_12
H5	I0_L8N_CC_12
D2	I0_L9P_CC_12
C2	I0_L9N_CC_12
K1	I0_L10P_CC_12
K2	I0_L10N_CC_12
G4	I0_L11P_CC_12
F4	I0_L11N_CC_12
C1	I0_L12P_VRN_12
B1	I0_L12N_VRP_12
G3	I0_L13P_12
F3	I0_L13N_12
F1	I0_L14P_12
E1	I0_L14N_VREF_12
J5	I0_L15P_12
J4	I0_L15N_12
H3	I0_L16P_12
J3	I0_L16N_12
H2	I0_L17P_12
J2	I0_L17N_12
E2	I0_L18P_12
F2	I0_L18N_12
G1	I0_L19P_12
H1	I0_L19N_12
K15	I0_L0P_13
L16	I0_L0N_13
L17	I0_L1P_13
K16	I0_L1N_13
K14	I0_L2P_13
L14	I0_L2N_13
M18	I0_L3P_13
L18	I0_L3N_13
L13	I0_L4P_13
M13	I0_L4N_VREF_13
P18	I0_L5P_13
N18	I0_L5N_13
M14	I0_L6P_13
N15	I0_L6N_13
P17	I0_L7P_13
R17	I0_L7N_13
M15	I0_L8P_CC_13
M16	I0_L8N_CC_13
N16	I0_L9P_CC_13
N17	I0_L9N_CC_13

XC5VLX30FF324

6. I/O Bank 18



7. Power and Ground

U?G		
D1	GND	VCC0_18
J1	GND	VCC0_18
P1	GND	VCC0_18
B2	GND	VCC0_18
M2	GND	VCC0_13
U2	GND	VCC0_13
E3	GND	VCC0_12
R3	GND	VCC0_12
H4	GND	VCC0_12
V4	GND	VCC0_12
A5	GND	VCC0_11
L5	GND	VCC0_11
D6	GND	VCC0_11
F6	GND	VCC0_11
P6	GND	VCC0_4
G7	GND	VCC0_4
J7	GND	VCC0_4
L7	GND	VCC0_3
U7	GND	VCC0_3
H8	GND	VCC0_3
F8	GND	VCC0_2
C9	GND	VCC0_2
N9	GND	VCC0_2
F10	GND	VCC0_1
T10	GND	VCC0_1
J11	GND	VCC0_1
B12	GND	VCC0_0
H12	GND	VCC0_0
K12	GND	VCC0_0
M12	GND	VCC0_0
E13	GND	VCCINT
J13	GND	VCCINT
P13	GND	VCCINT
H14	GND	VCCINT
V14	GND	VCCINT
A15	GND	VCCINT
L15	GND	VCCINT
D16	GND	VCCINT
P16	GND	VCCINT
B17	GND	VCCAUX
G17	GND	VCCAUX
U17	GND	VCCAUX
E18	GND	VCCAUX
K18	GND	VCCAUX
T5		N4
		K3
		N14
		M17
		G2
		F5
		C4
		J16
		F15
		C14
		U12
		P11
		D11
		A10
		V9
		R8
		B8
		B7
		T15
		R18
		L12
		J12
		K11
		H11
		L8
		J8
		K7
		K13
		G12
		M7
		H7
		J6

XC5VLX50FF324

8. Revision History

	Revision	Date	By	Comments
1	1.01	Jan 07, 2007	MD	Initial Release