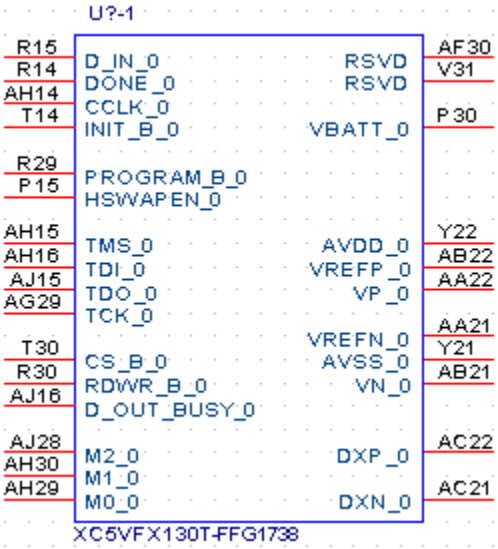
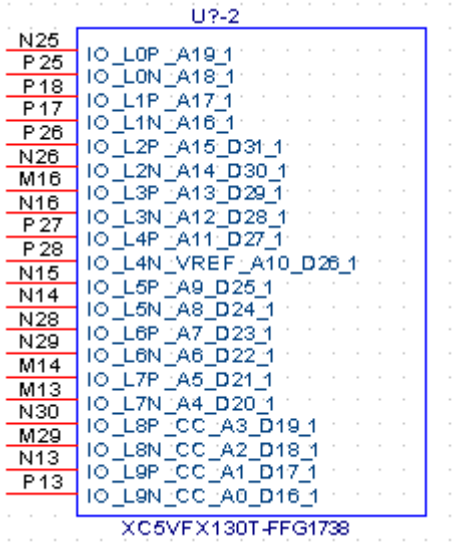
Schematic Symbol for XC5VFX130T-FFG1738

The symbol consists of 42 heterogeneous parts, each of them listed below:

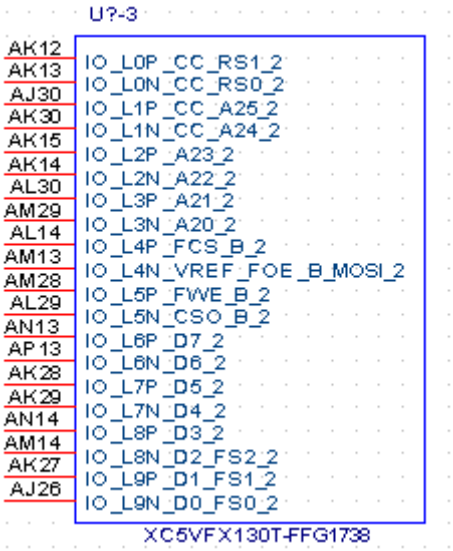
1. Programming Interface



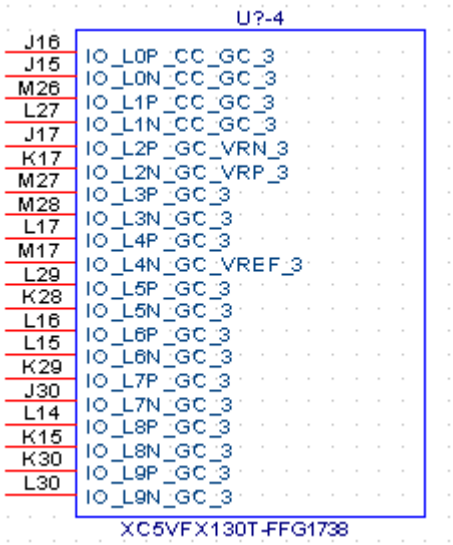
2. I/O Bank 1



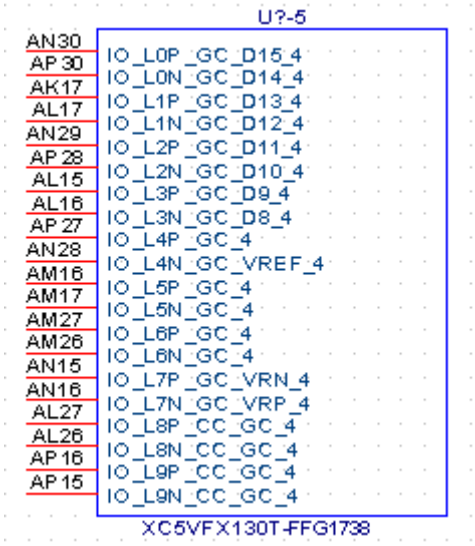
3. I/O Bank 2



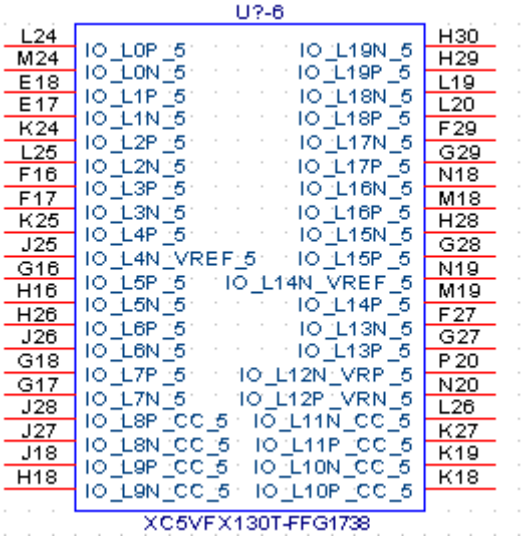
4. I/O Bank 3



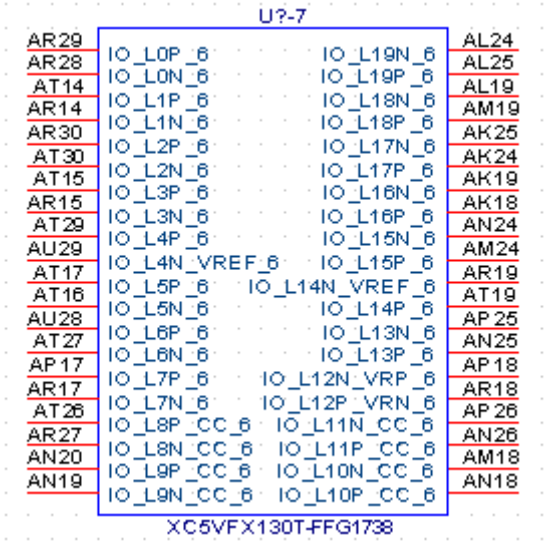
5. I/O Bank 4



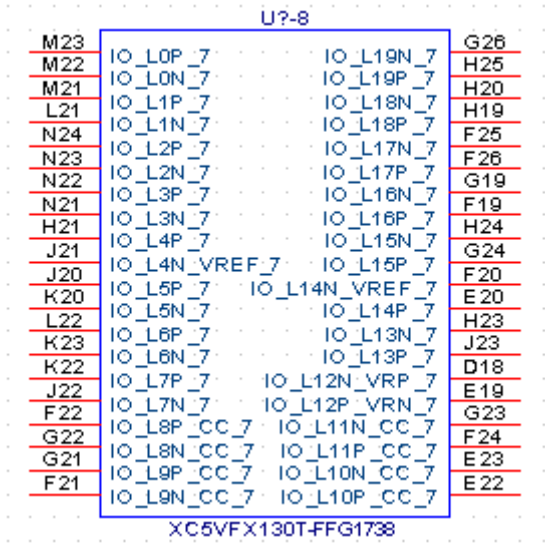
6. I/O Bank 5



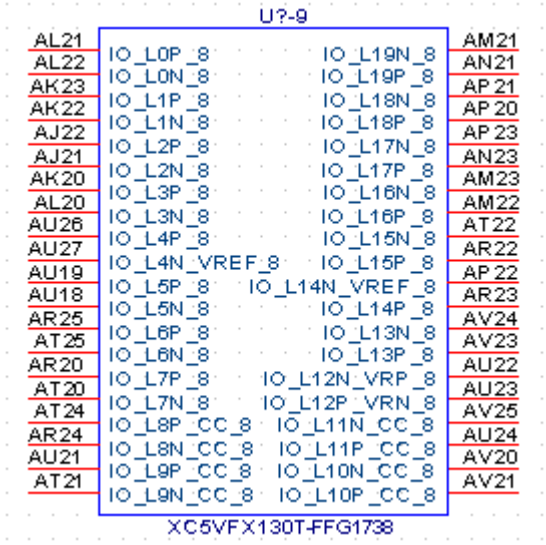
7. I/O Bank 6



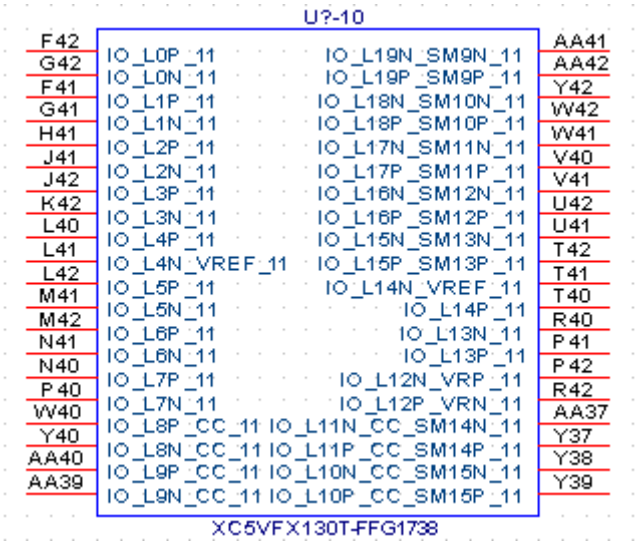
8. I/O Bank 7



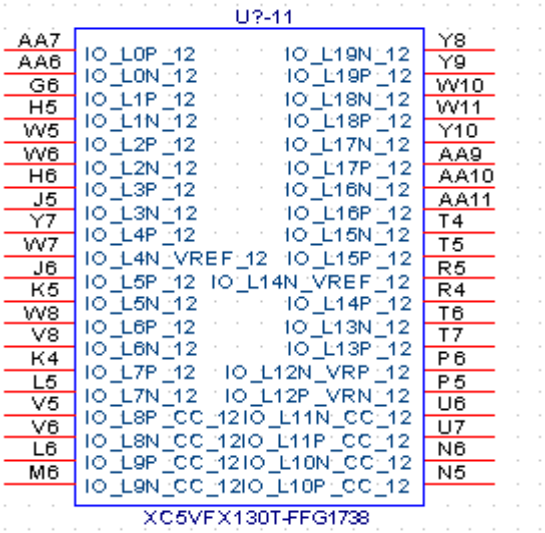
9. I/O Bank 8



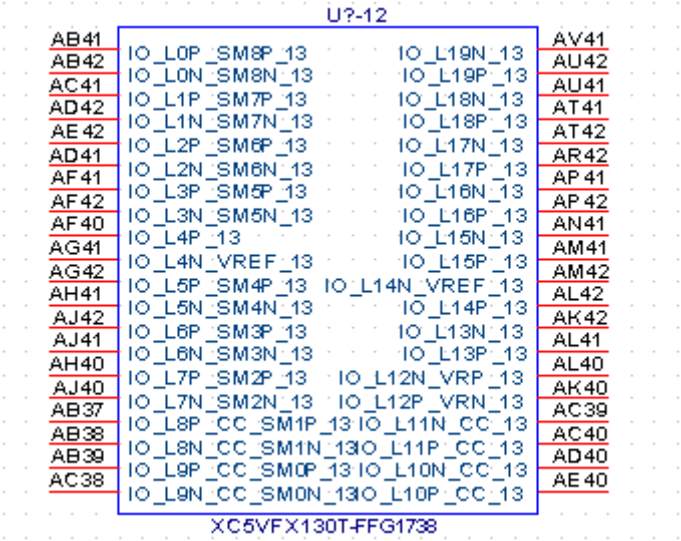
10. I/O Bank 11



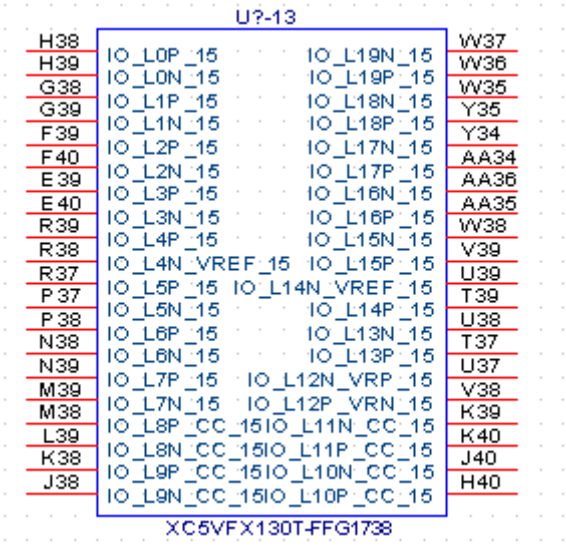
11. I/O Bank 12



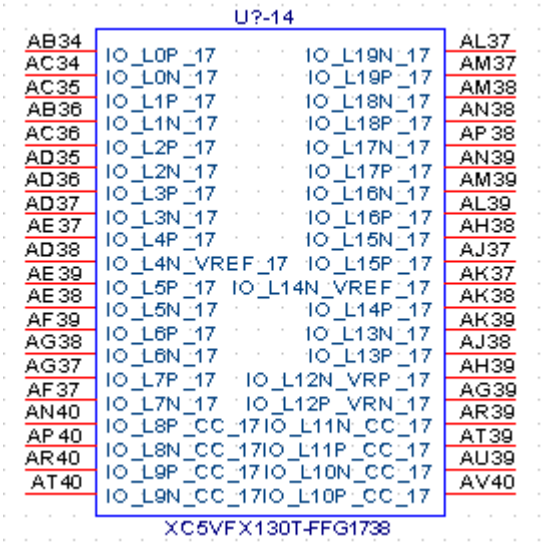
12. I/O Bank 13



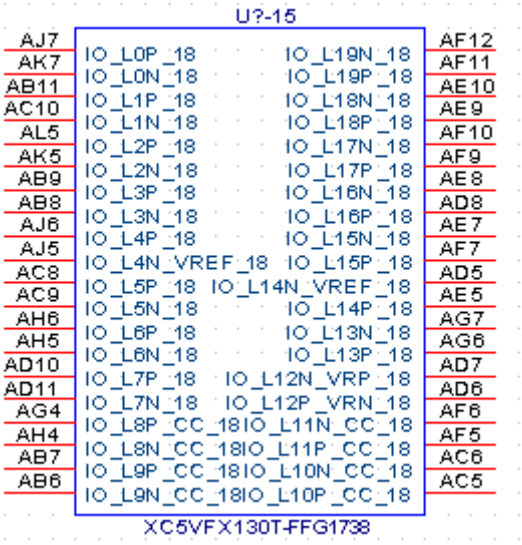
13. I/O Bank 15



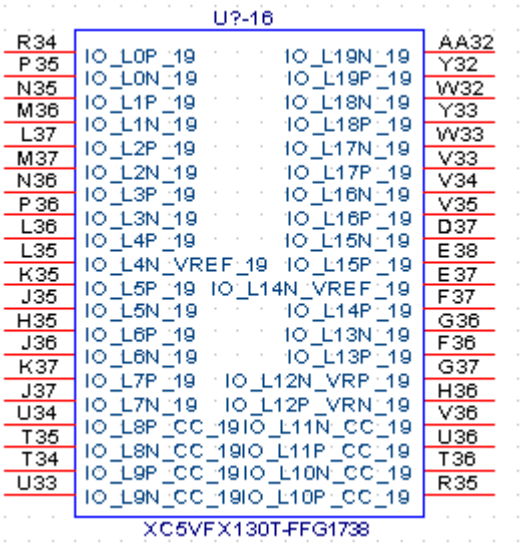
14. I/O Bank 17



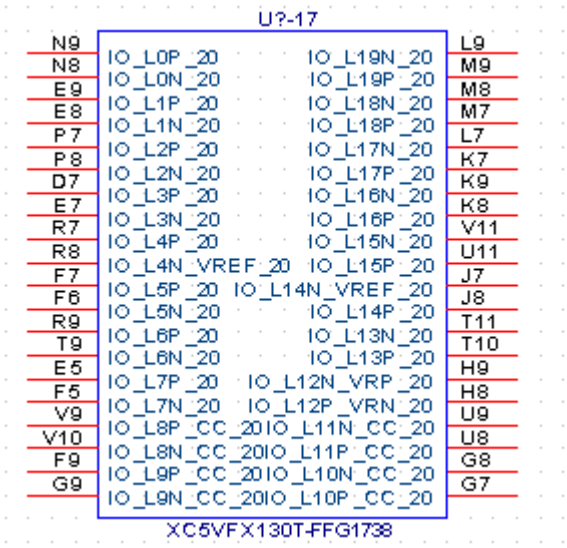
15. I/O Bank 18



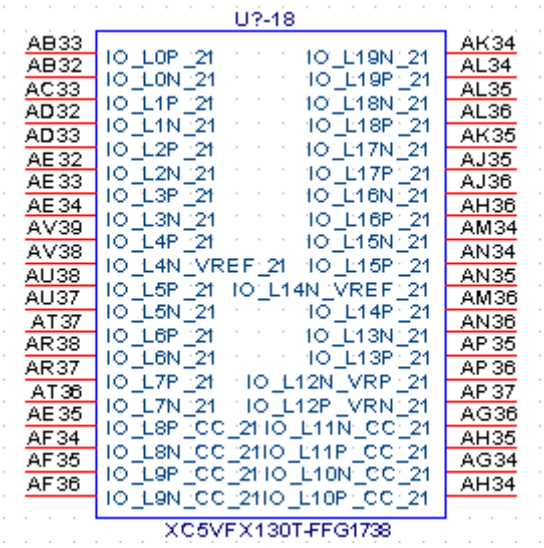
16. I/O Bank 19



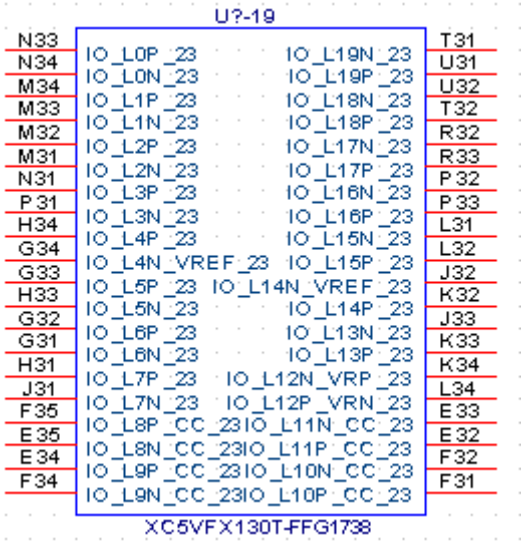
17. I/O Bank 20



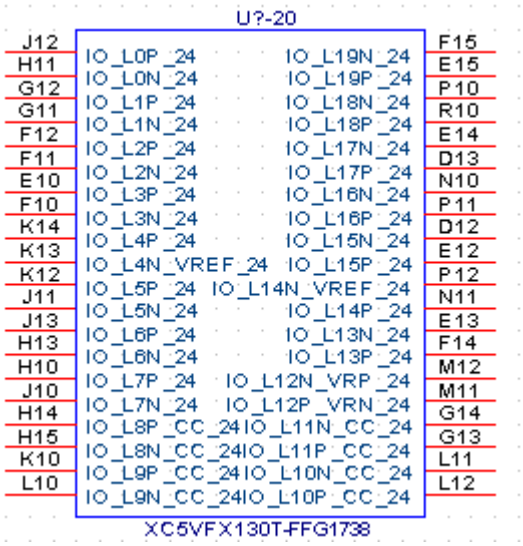
18. I/O Bank



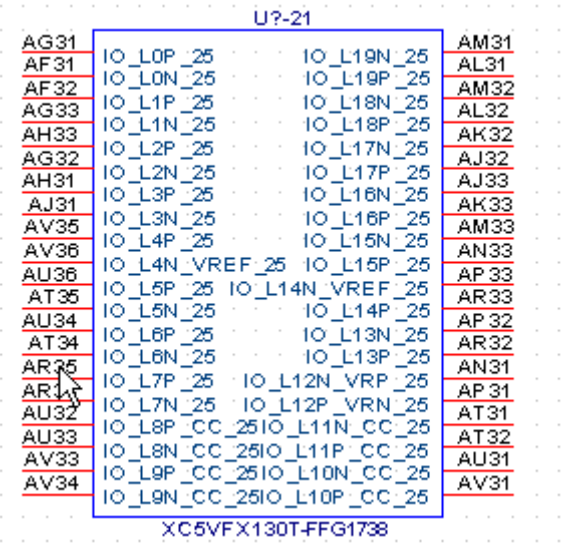
19. I/O Bank 23



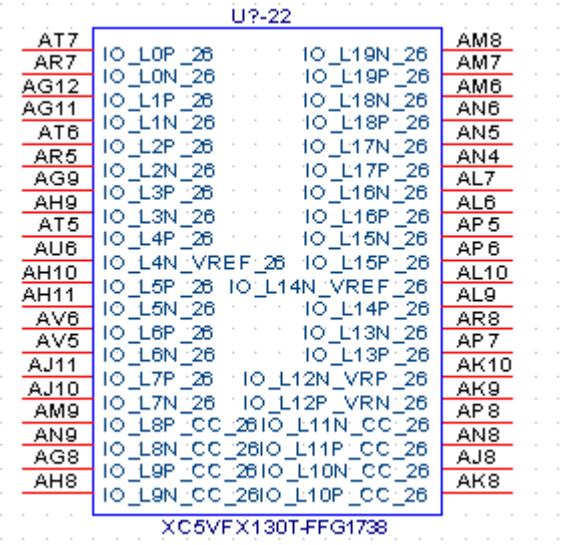
20. I/O Bank 24



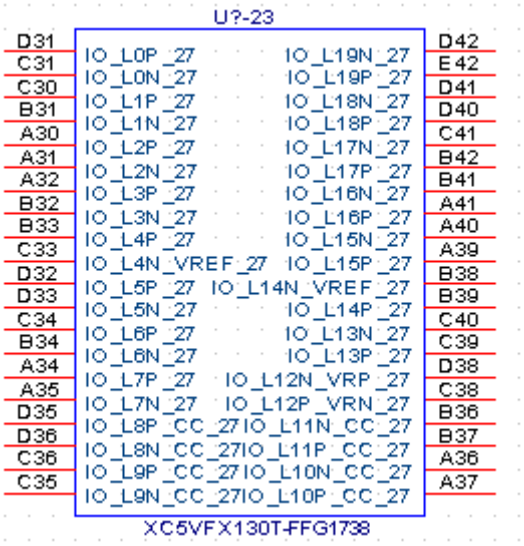
21. I/O Bank 25



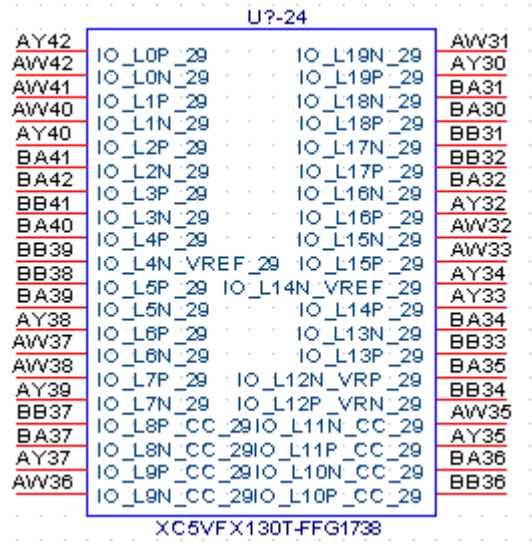
22. I/O Bank 26



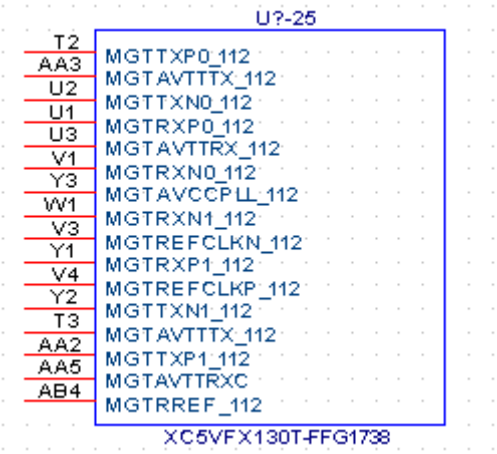
23. I/O Bank 27



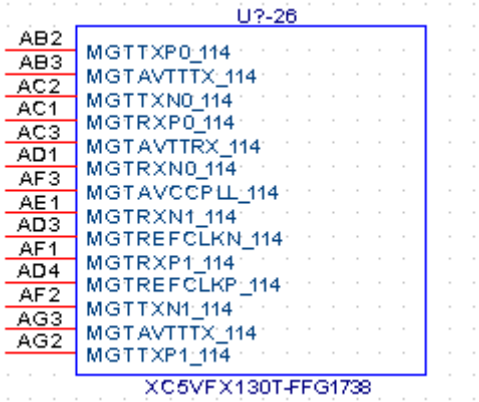
24. I/O Bank 29



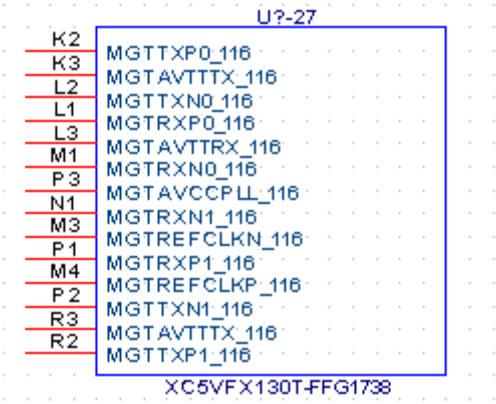
25. MGT 112



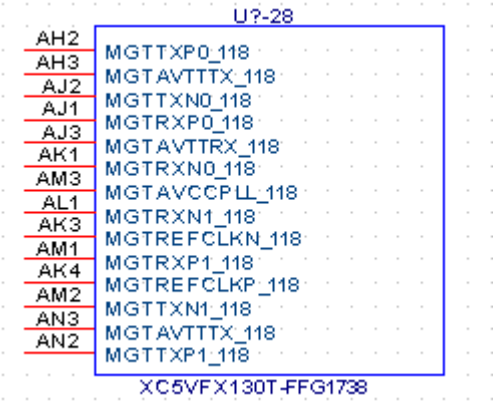
26. MGT 114



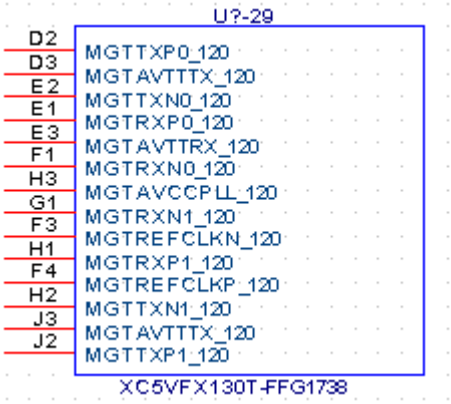
27. MGT 116



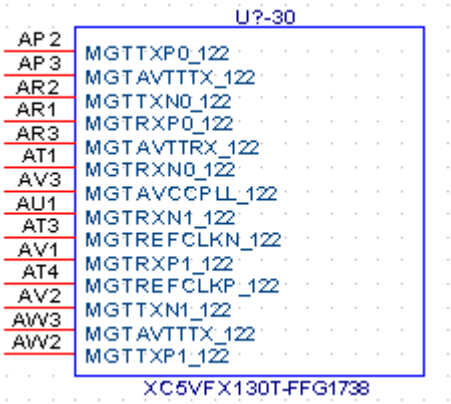
28. MGT 118



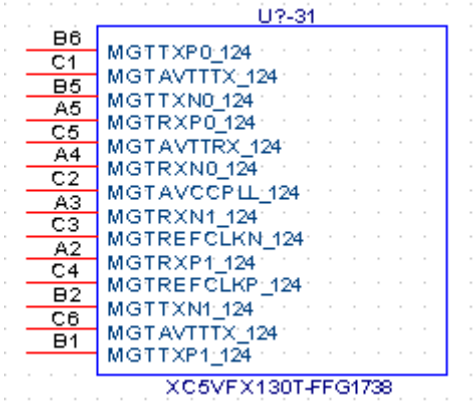
29. MGT 120



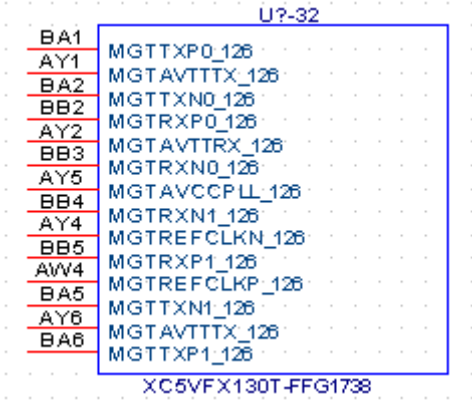
30. MGT 122



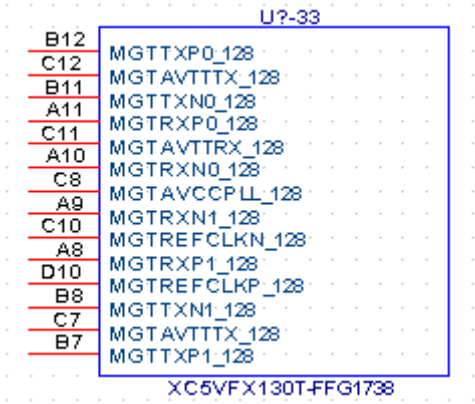
31. MGT 124



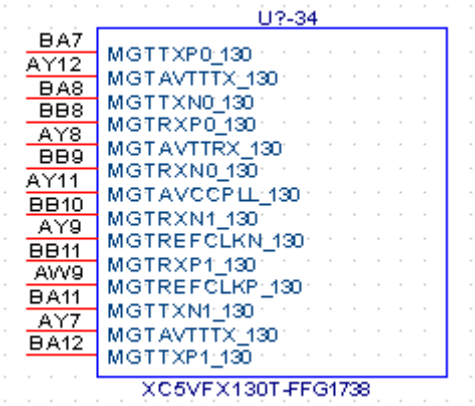
32. MGT 126



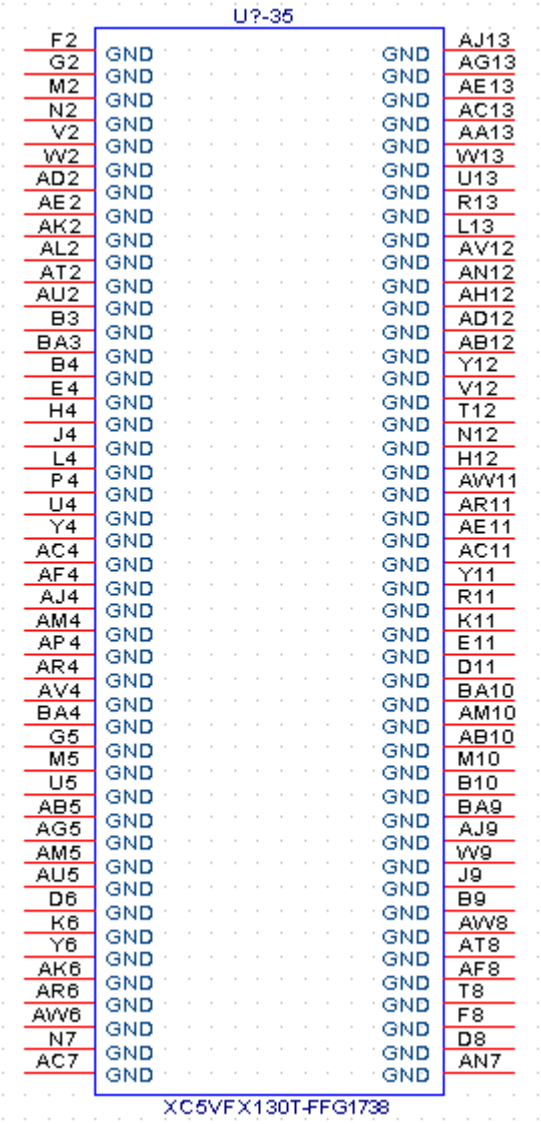
33. MGT 128



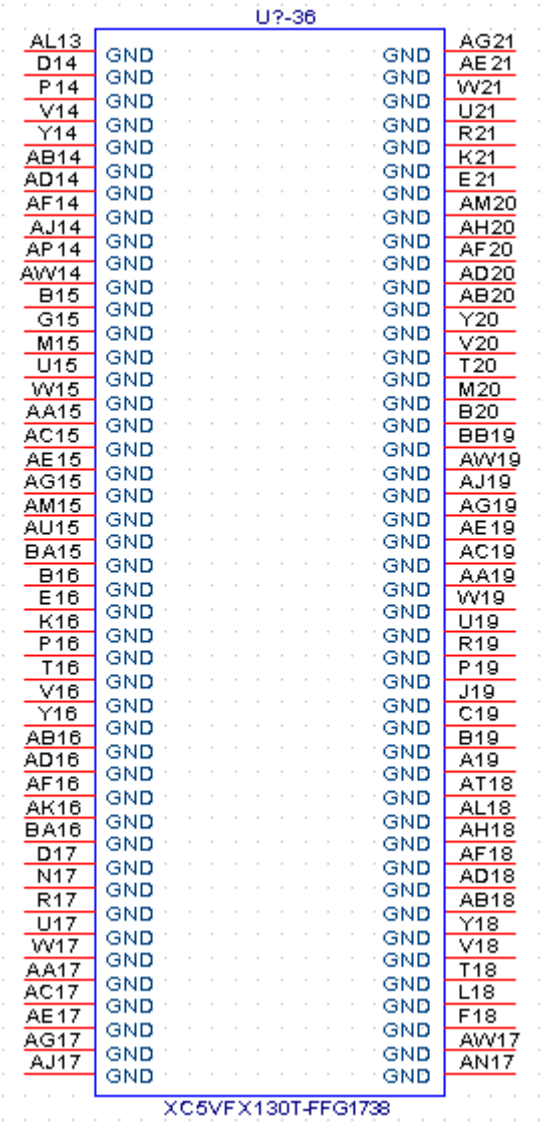
34. MGT 130


U?-34
BA7
MGTTXP0_130
AY12
MGTAVTTTX_130
BA8
MGTTXN0_130
BB8
MGTRXP0_130
AY8
MGTAVTTRX_130
BB9
MGTRXN0_130
AY11
MGTAVCCPLL_130
BB10
MGTRXN1_130
AY9
MGTREFCLKN_130
BB11
MGTRXP1_130
AW9
MGTREFCLKP_130
BA11
MGTTXN1_130
AY7
MGTAVTTTX_130
BA12
MGTTXP1_130
XC5VFX130T-FFG1738

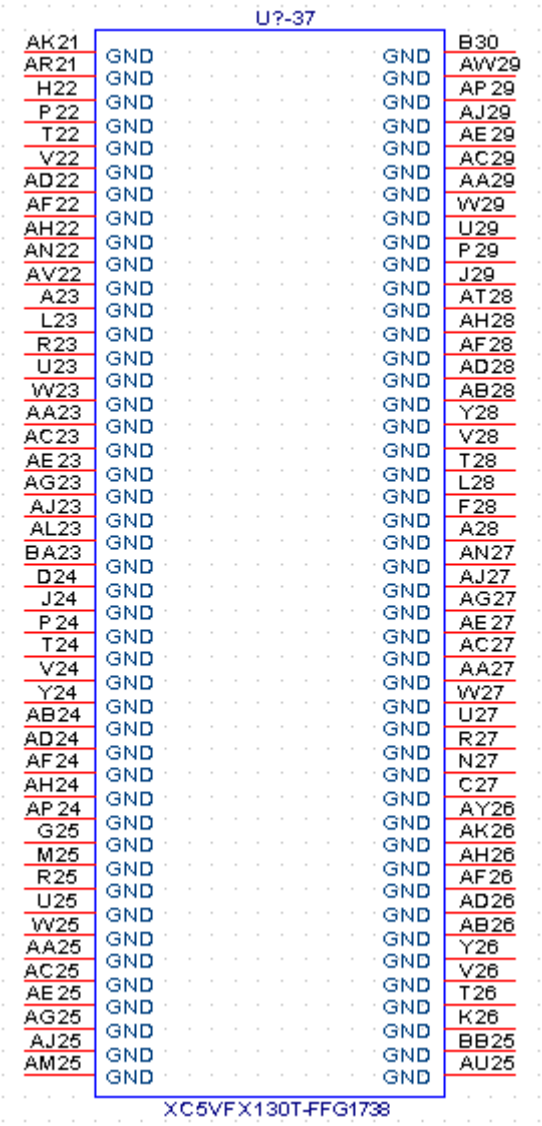
35. Power 1


U?-35
F2 GND
G2 GND
M2 GND
N2 GND
V2 GND
W2 GND
AD2 GND
AE2 GND
AK2 GND
AL2 GND
AT2 GND
AU2 GND
B3 GND
BA3 GND
B4 GND
E4 GND
H4 GND
J4 GND
L4 GND
P4 GND
U4 GND
Y4 GND
AC4 GND
AF4 GND
AJ4 GND
AM4 GND
AP4 GND
AR4 GND
AV4 GND
BA4 GND
G5 GND
M5 GND
U5 GND
AB5 GND
AG5 GND
AM5 GND
AU5 GND
D6 GND
K6 GND
Y6 GND
AK6 GND
AR6 GND
AW6 GND
N7 GND
AC7 GND
GND AJ13
GND AG13
GND AE13
GND AC13
GND AA13
GND W13
GND U13
GND R13
GND L13
GND AV12
GND AN12
GND AH12
GND AD12
GND AB12
GND Y12
GND V12
GND T12
GND N12
GND H12
GND AW11
GND AR11
GND AE11
GND AC11
GND Y11
GND R11
GND K11
GND E11
GND D11
GND BA10
GND AM10
GND AB10
GND M10
GND B10
GND BA9
GND AJ9
GND W9
GND J9
GND B9
GND AW8
GND AT8
GND AF8
GND T8
GND F8
GND D8
GND AN7
XC5VFX130T-FFG1738

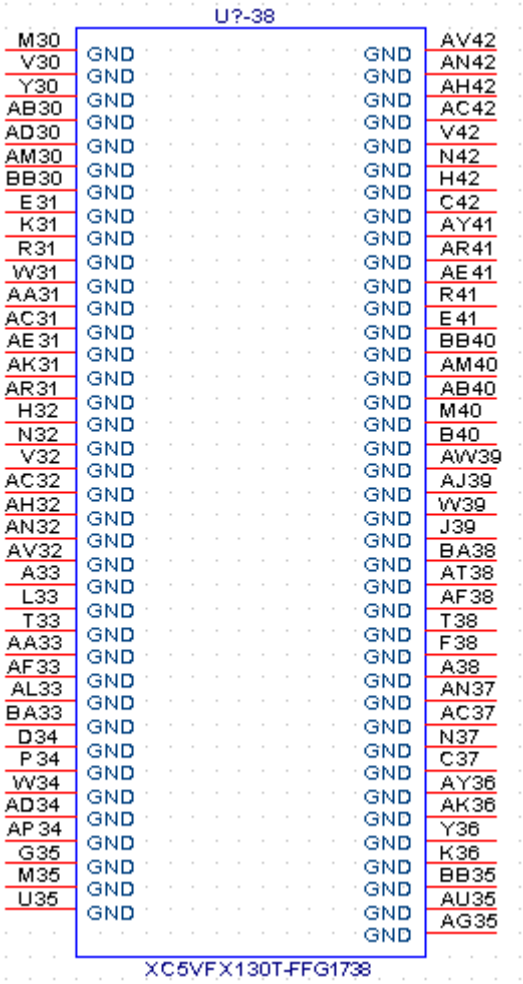
36. Power 2


U?-36
AL13 GND GND AG21
D14 GND GND AE21
P14 GND GND W21
V14 GND GND U21
Y14 GND GND R21
AB14 GND GND K21
AD14 GND GND E21
AF14 GND GND AM20
AJ14 GND GND AH20
AP14 GND GND AF20
AW14 GND GND AD20
B15 GND GND AB20
G15 GND GND Y20
M15 GND GND V20
U15 GND GND T20
W15 GND GND M20
AA15 GND GND B20
AC15 GND GND BB19
AE15 GND GND AW19
AG15 GND GND AJ19
AM15 GND GND AG19
AU15 GND GND AE19
BA15 GND GND AC19
B16 GND GND AA19
E16 GND GND W19
K16 GND GND U19
P16 GND GND R19
T16 GND GND P19
V16 GND GND J19
Y16 GND GND C19
AB16 GND GND B19
AD16 GND GND A19
AF16 GND GND AT18
AK16 GND GND AL18
BA16 GND GND AH18
D17 GND GND AF18
N17 GND GND AD18
R17 GND GND AB18
U17 GND GND Y18
W17 GND GND V18
AA17 GND GND T18
AC17 GND GND L18
AE17 GND GND F18
AG17 GND GND AW17
AJ17 GND GND AN17
XC5VFX130T-FFG1738

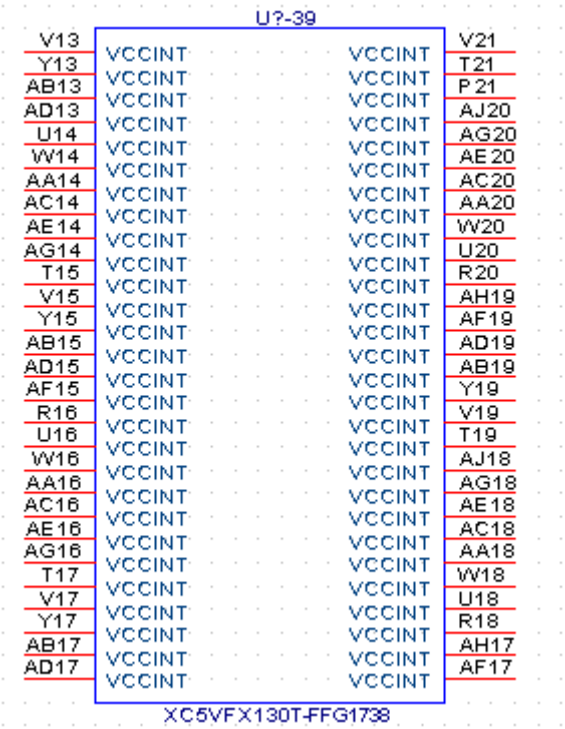
37. Power 3


U?-37
AK21 GND
AR21 GND
H22 GND
P22 GND
T22 GND
V22 GND
AD22 GND
AF22 GND
AH22 GND
AN22 GND
AV22 GND
A23 GND
L23 GND
R23 GND
U23 GND
W23 GND
AA23 GND
AC23 GND
AE23 GND
AG23 GND
AJ23 GND
AL23 GND
BA23 GND
D24 GND
J24 GND
P24 GND
T24 GND
V24 GND
Y24 GND
AB24 GND
AD24 GND
AF24 GND
AH24 GND
AP24 GND
G25 GND
M25 GND
R25 GND
U25 GND
W25 GND
AA25 GND
AC25 GND
AE25 GND
AG25 GND
AJ25 GND
AM25 GND
GND B30
GND AW29
GND AP29
GND AJ29
GND AE29
GND AC29
GND AA29
GND W29
GND U29
GND P29
GND J29
GND AT28
GND AH28
GND AF28
GND AD28
GND AB28
GND Y28
GND V28
GND T28
GND L28
GND F28
GND A28
GND AN27
GND AJ27
GND AG27
GND AE27
GND AC27
GND AA27
GND W27
GND U27
GND R27
GND N27
GND C27
GND AY26
GND AK26
GND AH26
GND AF26
GND AD26
GND AB26
GND Y26
GND V26
GND T26
GND K26
GND BB25
GND AU25
XC5VFX130T-FFG1738

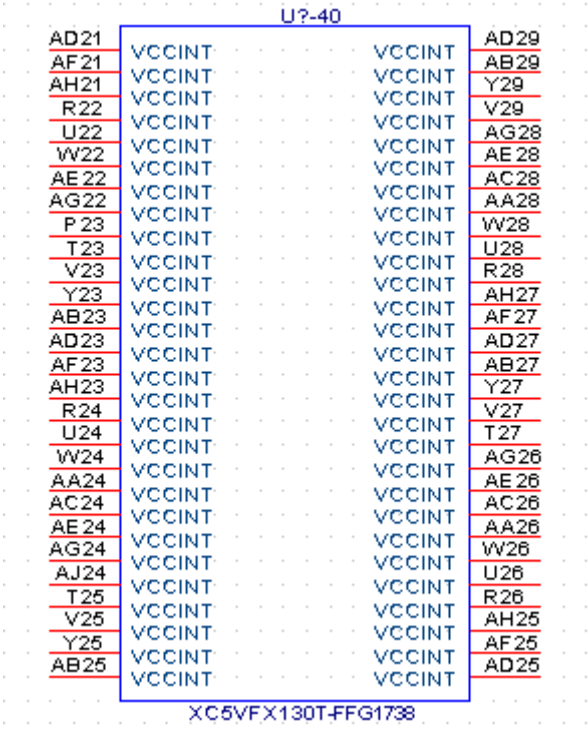
38. Power 4


U?-38
M30 GND
V30 GND
Y30 GND
AB30 GND
AD30 GND
AM30 GND
BB30 GND
E31 GND
K31 GND
R31 GND
W31 GND
AA31 GND
AC31 GND
AE31 GND
AK31 GND
AR31 GND
H32 GND
N32 GND
V32 GND
AC32 GND
AH32 GND
AN32 GND
AV32 GND
A33 GND
L33 GND
T33 GND
AA33 GND
AF33 GND
AL33 GND
BA33 GND
D34 GND
P34 GND
W34 GND
AD34 GND
AP34 GND
G35 GND
M35 GND
U35 GND
GND AV42
GND AN42
GND AH42
GND AC42
GND V42
GND N42
GND H42
GND C42
GND AY41
GND AR41
GND AE41
GND R41
GND E41
GND BB40
GND AM40
GND AB40
GND M40
GND B40
GND AW39
GND AJ39
GND W39
GND J39
GND BA38
GND AT38
GND AF38
GND T38
GND F38
GND A38
GND AN37
GND AC37
GND N37
GND C37
GND AY36
GND AK36
GND Y36
GND K36
GND BB35
GND AU35
GND AG35
XC5VFX130T-FFG1738

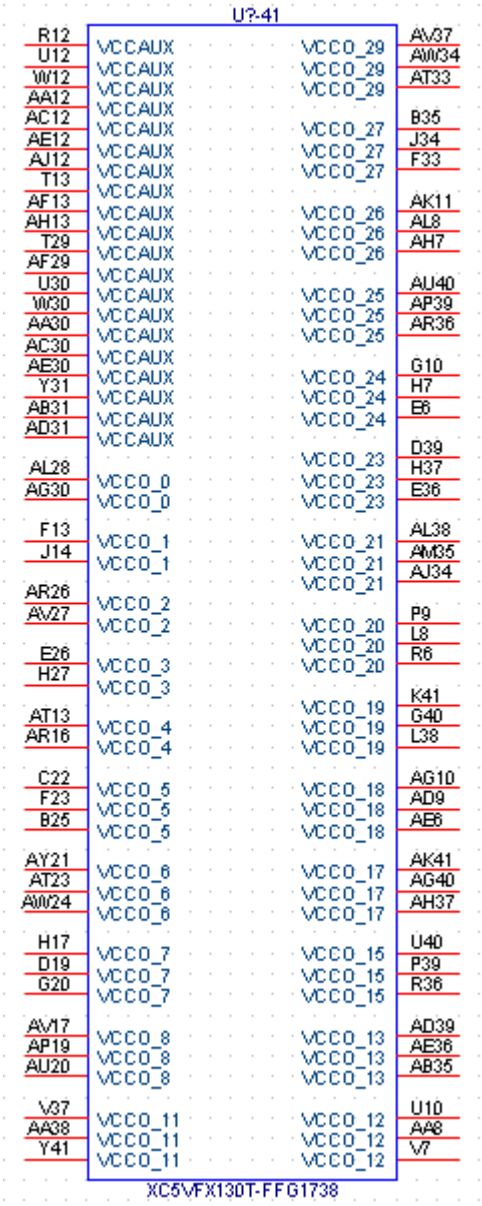
39. Power 5



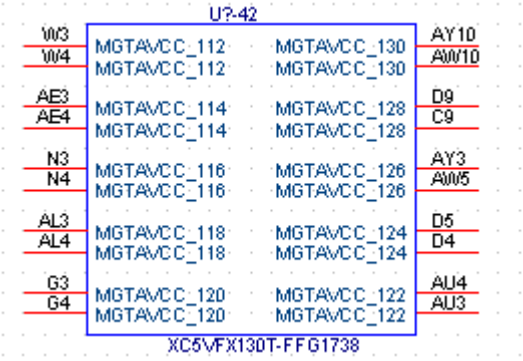
40. Power 6



41. Power 7


U?-41
R12 VCCAUX
U12 VCCAUX
W12 VCCAUX
AA12 VCCAUX
AC12 VCCAUX
AE12 VCCAUX
AJ12 VCCAUX
T13 VCCAUX
AF13 VCCAUX
AH13 VCCAUX
T29 VCCAUX
AF29 VCCAUX
U30 VCCAUX
W30 VCCAUX
AA30 VCCAUX
AC30 VCCAUX
AE30 VCCAUX
Y31 VCCAUX
AB31 VCCAUX
AD31 VCCAUX
AL28 VCCO_0
AG30 VCCO_0
F13 VCCO_1
J14 VCCO_1
AR26 VCCO_2
AV27 VCCO_2
E26 VCCO_3
H27 VCCO_3
AT13 VCCO_4
AR16 VCCO_4
C22 VCCO_5
F23 VCCO_5
B25 VCCO_5
AY21 VCCO_6
AT23 VCCO_6
AW24 VCCO_6
H17 VCCO_7
D19 VCCO_7
G20 VCCO_7
AV17 VCCO_8
AP19 VCCO_8
AU20 VCCO_8
V37 VCCO_11
AA38 VCCO_11
Y41 VCCO_11
VCCO_29 AV37
VCCO_29 AW34
VCCO_29 AT33
VCCO_27 B35
VCCO_27 J34
VCCO_27 F33
VCCO_26 AK11
VCCO_26 AL8
VCCO_26 AH7
VCCO_25 AU40
VCCO_25 AP39
VCCO_25 AR36
VCCO_24 G10
VCCO_24 H7
VCCO_24 B6
VCCO_23 D39
VCCO_23 H37
VCCO_23 E36
VCCO_21 AL38
VCCO_21 AM35
VCCO_21 AJ34
VCCO_20 P9
VCCO_20 L8
VCCO_20 R6
VCCO_19 K41
VCCO_19 G40
VCCO_19 L38
VCCO_18 AG10
VCCO_18 AD9
VCCO_18 AB6
VCCO_17 AK41
VCCO_17 AG40
VCCO_17 AH37
VCCO_15 U40
VCCO_15 P39
VCCO_15 R36
VCCO_13 AD39
VCCO_13 AE36
VCCO_13 AB35
VCCO_12 U10
VCCO_12 AA8
VCCO_12 V7
XC5VFX130T-FFG1738

42. Power 8



Notes:

1. **All the unconnected pins are not present on the symbol**
2. **All the pins and associated names were imported in Orcad from the Xilinx provided V5 ASCII files released on 12/19/2008.**
3. **All the I/O pins are assigned as “passive” to avoid warnings when running Orcad DRC.**
4. **If you plan on being able to migrate to a higher density component, please select the corresponding symbol for your design. Using the current one will not allow the direct migration due to the unconnected VCCO pins when migrating to the higher density component.**
5. **Please connect all the power pins in the design. This will allow proper operation of the FPGA device.**

Document Revision History

	Revision	Date	By	Comments
1	1.01	March 20, 09	MD	Initial Release